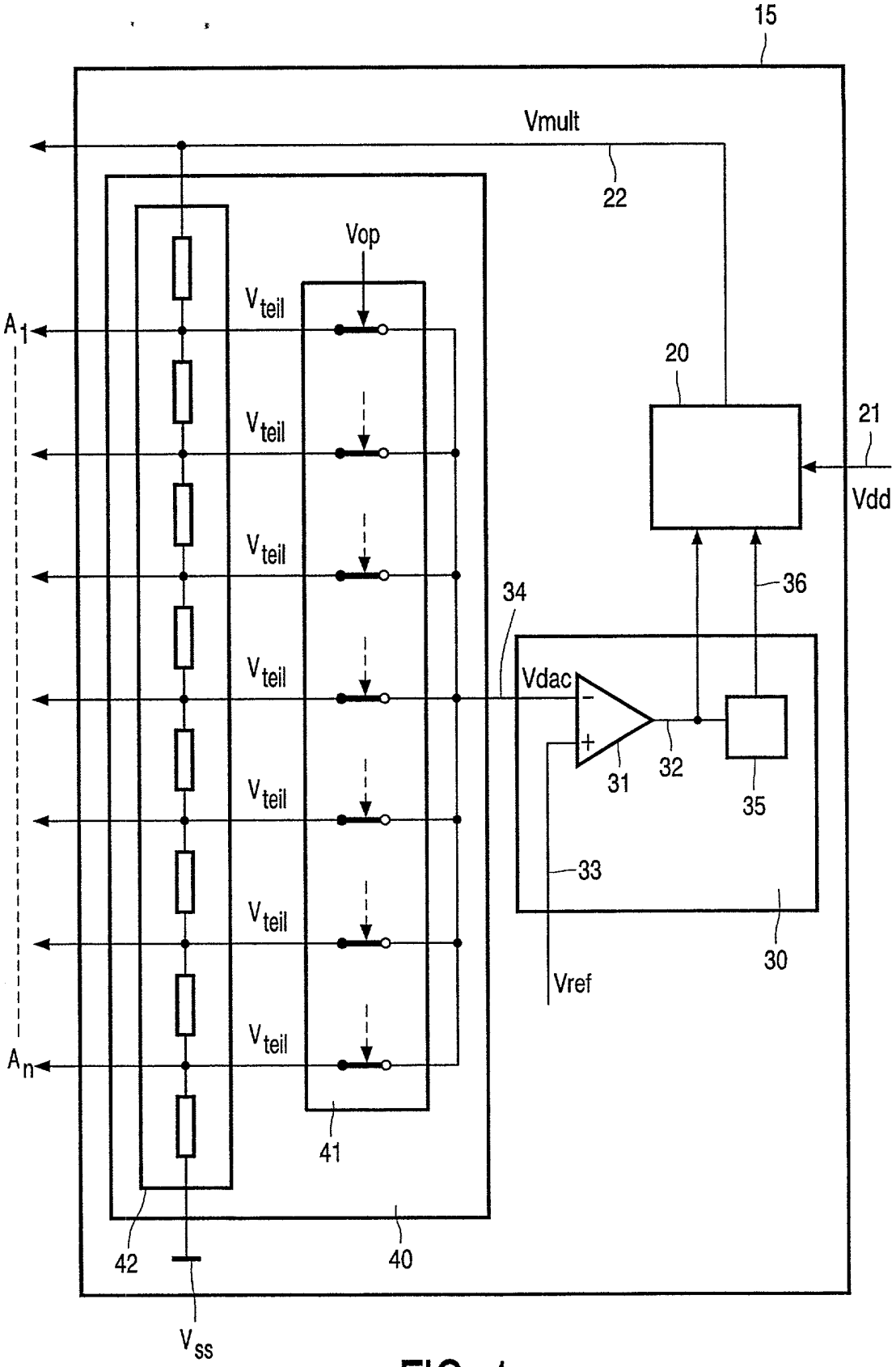
15
Vmult
22
Vop
V_{teil}
A_1
A_n
20
21
Vdd
36
34
Vdac
31
32
35
33
30
Vref
41
42
40
V_{ss}

FIG. 1

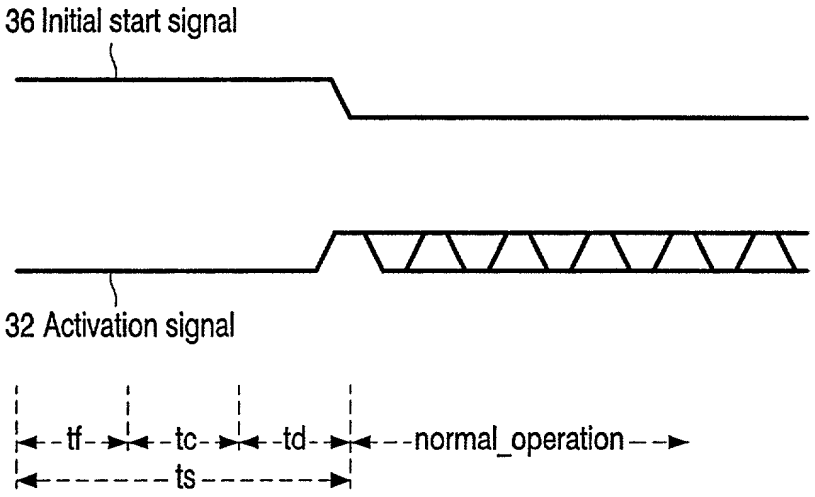
36 Initial start signal
32 Activation signal
tf
tc
td
normal_operation
ts

FIG. 2

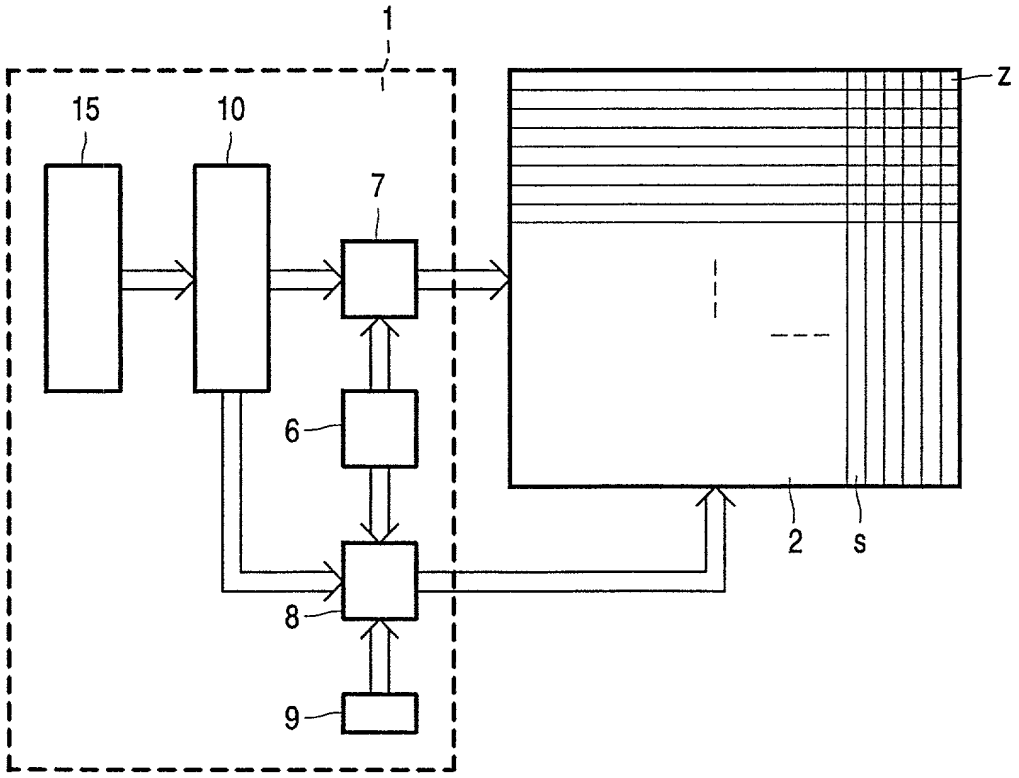
1
15
10
7
Z
6
2
s
8
9

FIG. 3

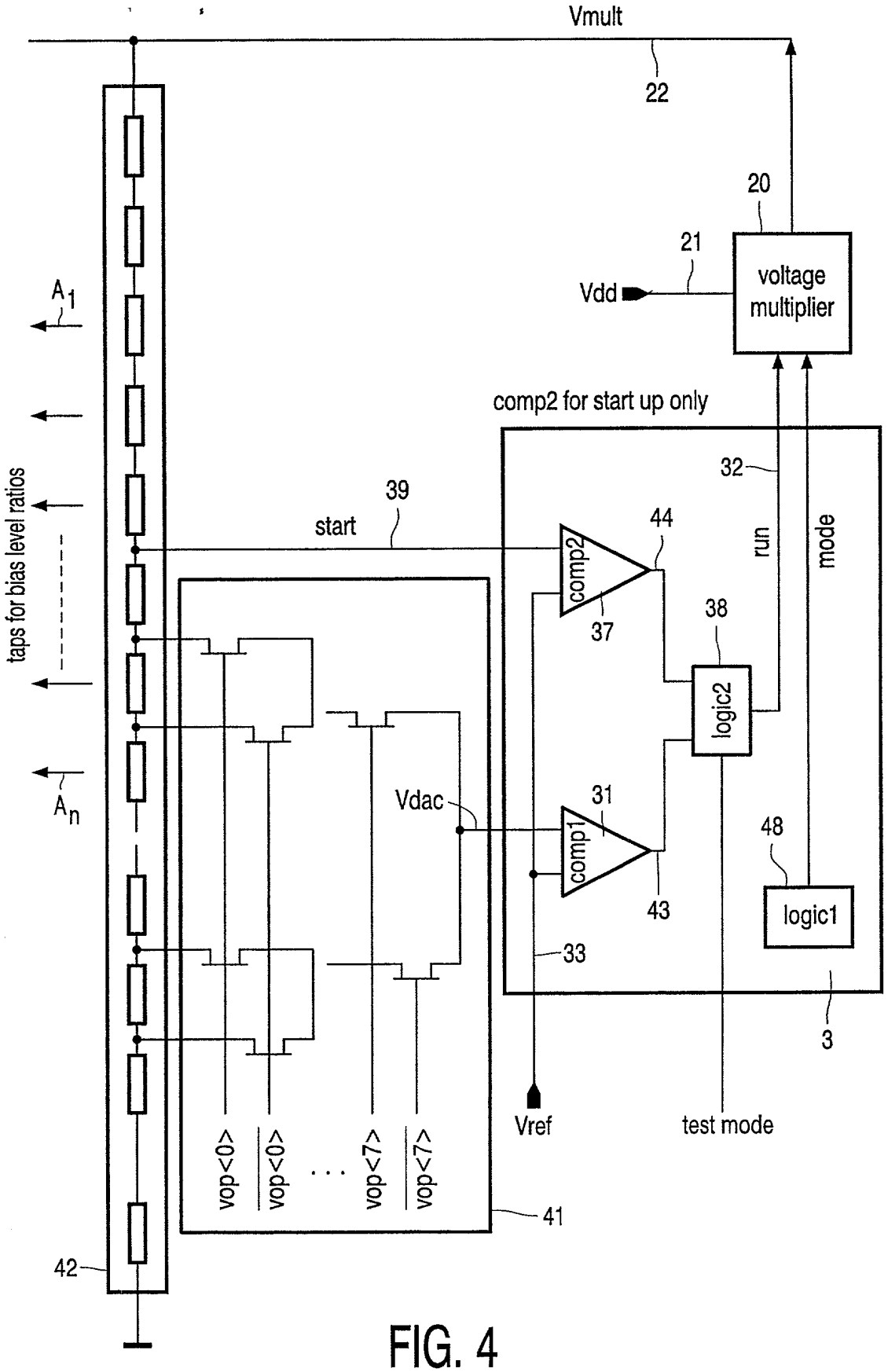
Vmult
22
20
21
Vdd
voltage multiplier
A1
An
taps for bias level ratios
comp2 for start up only
32
39
start
44
comp2
37
run
mode
38
logic2
Vdac
31
comp1
43
48
logic1
33
3
Vref
test mode
vop<0>
vop<0>
vop<7>
vop<7>
41
42

FIG. 4

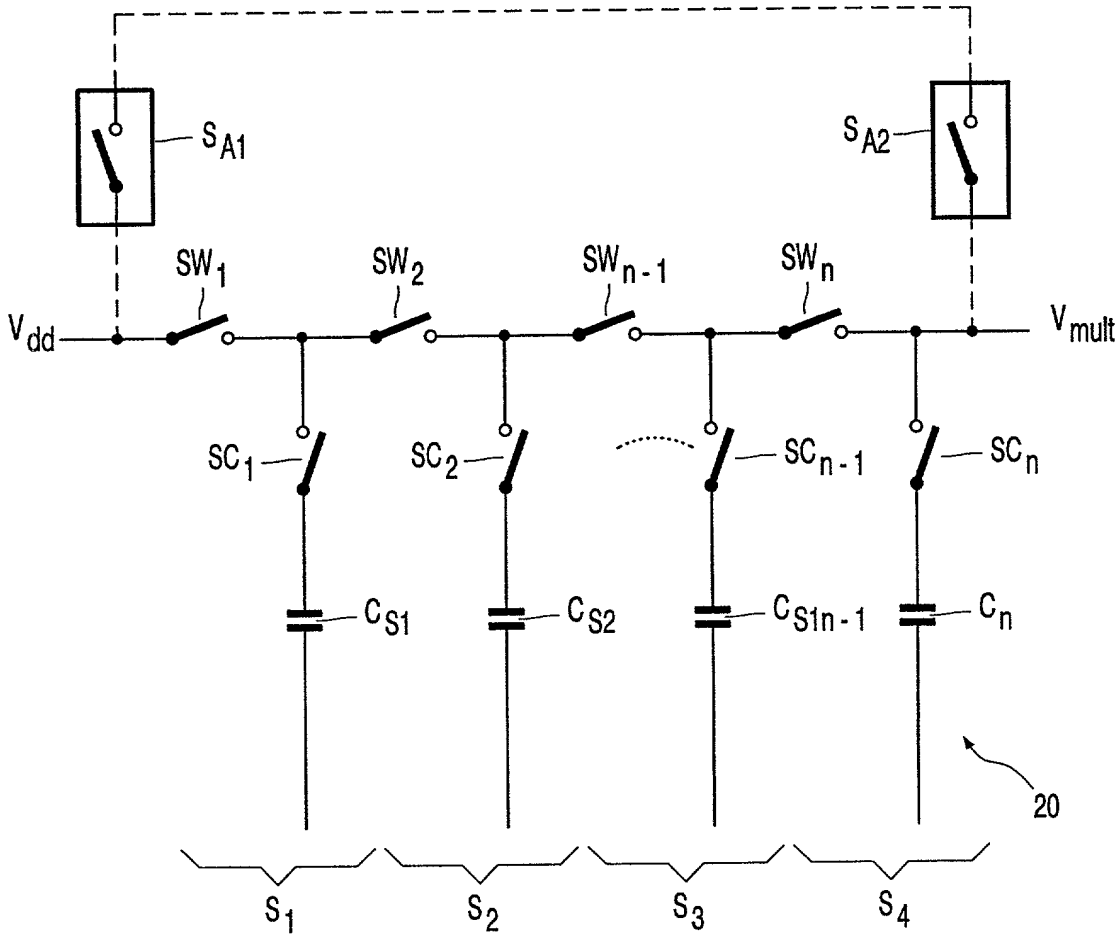
S_{A1}
S_{A2}
SW_1
SW_2
SW_{n-1}
SW_n
V_{dd}
V_{mult}
SC_1
SC_2
SC_{n-1}
SC_n
C_{S1}
C_{S2}
C_{S1n-1}
C_n
20
S_1
S_2
S_3
S_4

FIG. 5